Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-15. (Cancelled)

16. (new) Method to implement a column interleaving function, comprising the steps of:

providing a number of memories equal to the maximum number of columns in the interleaving function,

inputting a stream of data entities,

writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written,

performing selection and permutation on said memories, and

reading out said data entities in said permuted memories, in a memory-by-memory fashion.

17. (new) Method as in claim 16, wherein data entities in the input stream are first written into a register and when said register is filled, the step of writing into a memory is applied.

18. (new) Method as in claim 16, wherein said data entities are logical ones and zeros.

19. (new) Method as in claim 16, wherein said data entities are multiple bit words.

20. (new) Method as in claim 16, wherein said data entities are three bit words.

21. (new) Method as in claim 17, wherein said register is arranged to store each multiple bit word at one location in said memories.

22. (new) Method as in claim 16, wherein the number of columns used in the column interleaving function is changed on the fly, said number of columns not exceeding said maximum number of columns.

23. (new) A module for column interleaving comprising:

means for implementing a column interleaving function, wherein the means for implementing the column interleaving function comprises:

a number of memories equal to the maximum number of columns in the interleaving function,

means for inputting a stream of data entities,

means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written,

means for performing selection and permutation on said memories, and

means for reading out said data entities in said permuted memories, in a memory-by-memory fashion.

24. (new) A communication system device, comprising a module as in claim 23.

25. (new) A spread-spectrum communication apparatus comprising a module as in claim 23.

26. (new) An integrated circuit device comprising:

a module for column interleaving, said module comprising means for implementing a column interleaving function, wherein the means for implementing the column interleaving function comprises:

a number of memories equal to the maximum number of columns in the interleaving function,

means for inputting a stream of data entities,

means for writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written,

means for performing selection and permutation on said memories, and

means for reading out said data entities in said permuted memories, in a memory-by-memory fashion.

27. (new) A communication system device, comprising an integrated circuit device as in claim 26.

28. (new) A spread-spectrum communication apparatus comprising an integrated circuit device as in claim 26.

29. (new) A column interleaver, comprising a number of memories equal to the maximum number of columns desired in the interleaver and means to perform column selection and permutation.

30. (new) The column interleaver as in claim 29, further comprising a register.